

Testing and Evaluating the Quality-Level of Stratified Multichip Module Instrumentation

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Abstract

In this paper, approaches to testing and evaluating the quality-level (QL) of multichip module (MCM) instrumentations are proposed. A MCM is generally composed of a number of sets (or strata) of chips with different Known-Good-Yields (KGYS), so-called stratified, since each stratum is procured from a separate manufacturer. A stratified technique is proposed for testing MCM instrumentations. The proposed testing approach is accomplished in the presence of uneven known-good-yield (KGY) for MCMs consisting of different sets (or strata) of chips. This approach referred to as the lowest yield-stratum first-testing (LYSFT) considers the unevenness of KGY between strata for testing the chips and improving the QL. For comparison purposes, exhaustive testing (ET), random testing (RT) and random stratified testing (RST) are also evaluated by using a Markov-chain model. A Markov-chain model is used to analyze the quality-levels of these testing approaches and is solved analytically in $O(SN^3)$ for the LYSFT (where S is the number of strata and N is the number of chips in the MCM). A cost model is proposed and shown as figure of merit and shown to relate the defect-level with the number of tests performed. Parametric results show that the LYSFT dramatically outperforms RT and RST for improving the quality-level. A considerable reduction in tests can be achieved by the LYSFT at a very small loss in quality-level compared with ET. Based on the proposed cost model, it is also shown that the LYSFT is the most cost-effective strategy.

1 Introduction

A MCM instrumentation is generally composed of a number of sets (or strata) of chips with a different KGY; each stratum is procured from a separate manufacturer. Without loss of generality the variance in KGY between chips in a stratum is usually *small*, while variance between strata can be *larger* than between chips in a stratum. In this paper this is referred to as *stratification*. In Figure (1), the chips of the same type are assumed to constitute a *stratum* (i.e. there are 5 strata by definition of stratum in this paper). Chips of the same type are procured from the same manufacturer with a uniform KGY (i.e. a low variance in their KGY). A heterogeneity in KGY (i.e. high variance in KGY) between chips in different strata is assumed as different manufacturers can be involved. This characteristic of MCMs is employed to enhance the performance of RT and reduce the number of tests, thus, ultimately reducing the cost of testing each stratum based on its KGY value. This process is referred to as *stratified testing*, i.e. a testing process based on stratification. The overhead for chip sampling based on the KGY of each stratum is $O(S)$ (where S is the number of strata in the MCM), not $O(N)$ as in [13] as based on the KGY of each individual chip (where N is the number of chips on the MCM). Therefore, testing is accomplished by exploiting the homogeneity between chips in each stratum and the heterogeneity between strata.

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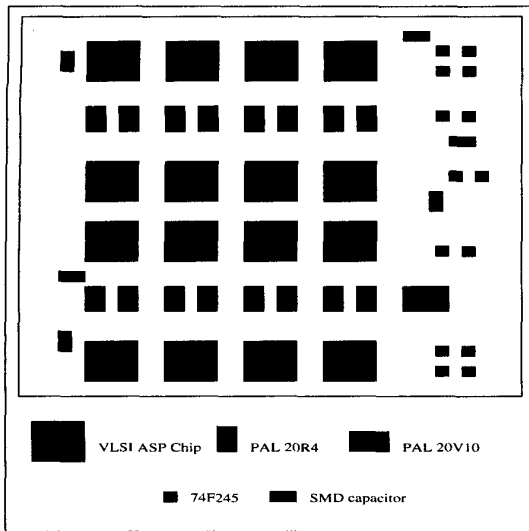


Figure 1. A MCM instrumentation composed of discrete VLSI chips

low variance in their KGY). A heterogeneity in KGY (i.e. high variance in KGY) between chips in different strata is assumed as different manufacturers can be involved. This is referred as *stratification*.

Exhaustive testing (ET) [13, 1, 4, 20, 16, 15] and *random testing* (RT) are defined as the process which tests every chip, and the process which tests only a number of randomly sampled chips in the MCM, respectively (note that chip sampling is the process of selecting a chip for testing). Therefore, conventional exhaustive and random testing [7, 8, 11, 12] for a VLSI chip can be extended to the scenario of multiple chips as applicable to systems such as MCMs. Also, *random stratified testing* (RST) is introduced in this paper; RST is defined as the process which tests chips from randomly sampled sets of equal chips (or stratum) on the MCM first.

The *unevenness* of FC in RT occurs between strata, i.e. different numbers of chips are sampled and tested in each stratum based on the KGY. Hence, a *lowest-yield-stratum first-testing* (LYSFT) approach is proposed and evaluated as basic criterion for *stratified testing*. A qualitative comparison between testing strategies for MCMs is summarized in Table (1). In Table (1), each strategy is ranked as follows: 1 (4) stands for the strategy which achieves the highest (lowest) QL; the strategy which requires the shortest (longest) time; and the strategy which utilizes the smallest (largest) number of tests.

The main objective of this paper is to demonstrate the feasibility of stratified testing (i.e. the LYSFT) for MCMs by evaluating the QL and cost reduction based on a cost-

Table 1. Qualitative comparison between testing strategies for MCMs

Comparison	LYSFT	RT	RST	ET
QL	2	4	3	1
Test time	3	1	2	4
Test length	1	1	1	2

model under uneven KGY between strata. This is used to achieve cost-effective testing compared with RT and RST (for improving the QL) and ET (by reducing the number of tests at an acceptable small loss of QL).

The organization of this paper is as follows. In the following section, the Lowest Yield Stratum First Testing (LYSFT) approach is introduced. Section 3 describes the analytical approach for evaluating the LYSFT approach based on a novel Markov model. In the final section, discussion and conclusions are presented.

2 Testing MCM Instrumentation

The number of sampled chips in each stratum for RT is commonly assumed to be even as no discrimination in the selection process is employed. A serious loss in QL could result by testing every chip with an even weight, i.e. excessive testing of high KGY chips and a lack of testing for low KGY chips may occur. Hence, the LYSFT is proposed for selection in testing a stratum.

In the proposed LYSFT, given the number of tests and hardware overhead, testing of the chips is based on the KGY of the stratum. LYSFT is a very straightforward approach that greedy (first) allocates and samples chips from the stratum with the lowest KGY. Thereby, the chips in the stratum with the highest KGY are selected last for testing. The main characteristics of this approach are as follows.

1. The time overhead for stratifying chips in the given MCM is negligible (i.e. $O(S)$, where S is the number of strata).
2. Due to the separate procurement of chips in MCMs, variance of the KGY is assumed to be small in a stratum and large between strata [2].
3. For non-sampled chips, the probability to escape in testing is given by the probability to be bad (i.e. $1 - Y$, as Y is the KGY of a chip). Hence, the impact of escaping on the QL for chips with a low KGY can be significant. The main objective of the LYSFT is to reduce the overall probability of escaping for low KGY chips by testing low KGY chips greedy (first).

Given Y , C and S , the proposed approach consists of the following chip-level steps.

1. A good chip is tested as good, with probability Y ;
2. A bad chip is tested correctly as bad, with probability $\bar{Y}C$;
3. A bad chip is tested incorrectly as escaped, with probability $\bar{Y}\bar{C}$;
4. All the bad chips not selected for testing escape, with probability $\bar{Y}$ and all the good chips not selected for testing do not affect the QL.

As shown in previous work [13], testing, and mounting during assembly are stochastic processes. Also, the random chip selection process within a stratum and testing on a stratum by stratum basis (in an arbitrary order) are stochastic. Hence, a Markov based model can be appropriately formulated for analyzing the QL of the LYSFT. Using the proposed Markov model, it is possible to evaluate the effect of the LYSFT on the QL during assembly. One of the objectives of this paper is therefore, to find an effective partial testing strategy for MCMs under uneven KGY between strata [2].

3 Evaluating the Quality-Level of MCM Instrumentation

In the proposed Markov model, a state (i, j, k, s) for the stochastic processes of testing and mounting each chip is defined as follows : i out of N_s chips in stratum s (where N_s is the number of chips in stratum s and s is the stratum currently under test) are tested-mounted-as-good, j out of N_s chips in stratum s are tested-mounted-as-bad and k chips out of $\sum_{c=1}^{s-1} N_c + i + j + k$ are tested-mounted-as-escaped up to $s - 1$ strata and up to the current chip in stratum s under testing. Note that the value of k is cumulative throughout the whole strata, thereby excluding all the states with chips escaped in the testing process.

At each state, there is only one untested chip for $N_s > i + j + k$ and $S \geq s$ (where S is the number of strata in the MCM). The defect level (DL) of the MCM is given by the sum of the probabilities of the states in which $i + j + k = N$, $k > 0$ and $s = S$. The value of k is obviously a function of both the KGY and FC (under the assumption of perfect diagnosis and no repair).

State transitions take place every time a chip is tested and mounted. Tests are independent for RT, commonly by using an appropriate hardware arrangement [20]. The state transition rates for every state when the current chip is selected (sampled or not) for testing, are given in Figures (2) and (3), respectively.

From state (i, j, k, s) , ($N > i + j + k$ and $S \geq s$) in Figure (2), three transitions can occur and are defined as follows :

1. A just-mounted chip is tested, mounted as good, thus driving the system into state $(i + 1, j, k, s)$, with probability Y .
2. A just-mounted chip is tested as bad, thus driving the system into state $(i, j + 1, k, s)$, with probability $\bar{Y}C$. The implication of this transition probability is that a chip is correctly tested as bad only if the testing process detects all faults with probability C .
3. A faulty chip is tested, mounted as good, thus driving the system into state $(i, j, k + 1, s)$, with probability $\bar{Y}\bar{C}$. This implies that a chip can be faulty, with probability $\bar{Y}$ and the testing process fails in detecting all faults, with probability $\bar{C}$.

From state (i, j, k, s) , ($N > i + j + k$ and $S \geq s$) in Figure (3), two transitions can occur and are defined as follows :

1. A just-mounted good chip is not tested and mounted (as good), with probability Y .
2. A just-mounted bad chip is not tested, but mounted (as good), with probability $\bar{Y}$.

$(1, 0, 0, s + 1)$, $(0, 1, 0, s + 1)$ and $(0, 0, 1, s + 1)$. So, the states with $k > 0$ are effectively excluded from the states with $k = 0$, to simplify the calculation of QL.

The overall QL and DL of a MCM using the LYSFT can be derived as a function of the KGY (Y), the FC (C) and the number of chips and sampled chips in each stratum. These are given as follows

$$QL = \sum_{i+j=N, j \leq t_s} P(i, j, 0, S), \quad (1)$$

$$DL = 1 - \sum_{i+j=N, j \leq t_s} P(i, j, 0, S) = 1 - QL, \quad (2)$$

where S is the number of the last stratum tested and t_s is the number of samples for the last stratum. The time complexity (T) of this algorithm is $O(SN^3)$.

The QL of RST can be evaluated as follows.

$$QL = \sum_{i=1}^{sset} \frac{1}{sset} ql_i, \quad (3)$$

where $sset$ is the number of all the possible sets of stratum sampling. This is given by ${}_S C_r R$ where r is the quotient of $\frac{SPL}{ssize}$, ${}_S C_r = \frac{S!}{r!(S-r)!}$, and SPL and $ssize$ are the

number of total chips and the number of chips in each stratum to be sampled (note that in this paper *ssize* is assumed to be the same for each stratum), respectively. R is the number of all the possible combinations for allocating samples to the last stratum (i.e. less than the whole stratum can be allocated for the last sampled stratum). Due to randomness, the probability for each stratum to be sampled is $\frac{1}{ssize}$. ql_i is the QL of the chips sampled for the i 'th combination.

The overall DL of the ET with uneven KGY is calculated using the same Markov-model and the same algorithm of [13] with a fixed value for the FC.

In Figures (4), the DL of each strategy is plotted versus number of samples and variance of KGY between strata (for a given value of KGY of the MCM). The DL increase of the LYSFT versus ET is plotted in Figure (5). To evaluate the DL ratio (%) (i.e. $\frac{DL_{RT}}{DL_{LYSFT}}$) of the RT compared to the LYSFT, its increase is plotted in Figure (6) over the whole range of sample sizes. However, the DL (or QL) is not fully representative as a sole figure of merit for testings MCMs during assembly phase. Hence, a new cost model as figure of merit is introduced to relate the cost to the DL and the number of chips to test. This is given as follows :

$$Relative_Cost(K) = \frac{DL_i - DL_{exh}}{K}, \quad (4)$$

where $K = N_{exh} - N_i$, DL_i and DL_{exh} are the DL of the i th testing strategy and ET, respectively; and N_{exh} and N_i are the number of chips tested by the i th testing strategy and ET, respectively. Thus, it is referred to as the *Relative.Cost*, i.e. the cost relative to the DL and the number of tests for the ET. The cost of each strategy is shown in Figure (7) based on *Relative.Cost* in equation (4).

4 Discussion and Conclusions

This paper has proposed new testing and evaluation approaches for MCM instrumentations to achieve a high QL and to save a significant number of tests during assembly. In this paper, it has been shown that the stratification of MCMs due to the different nature and procurement of the chips can be exploited for testing. Unlike conventional RT, the proposed approach referred to as the LYSFT, takes into account the uneven KGY due to stratification to improve the QL (compared with conventional RT and RST). A Markov model has been proposed to evaluate the proposed approach under the assumption of independent failure of chips in the MCM.

In the LYSFT approach, the effect of the uneven KGY between strata has been analyzed with respect to the variance of KGY and the sample size. It is shown that the LYSFT approach significantly outperforms conventional RT and RST, and is competitive even with a conventional

ET at a very small loss in QL by greedy (first) testing the chips in the stratum with lower KGY. Also, a new figure of merit to relate the cost of the testing process to the DL and the number of samples is proposed. This is a function of cost relative to the ET; the cost of the LYSFT is shown to outperform RT and RST for a given level of sample size.

Extensive parametric and cost analysis has been performed for comparing RT, RST and ET. From the results of the parametric analysis, the LYSFT is shown to be more effective under a high MCM yield and high variance of KGY between strata. The performance of the proposed LYSFT can outperform RT by about 45%-80% improvement in QL and is viable even compared with a conventional ET for a significant reduction in the amount of tests for an acceptable low loss in QL.

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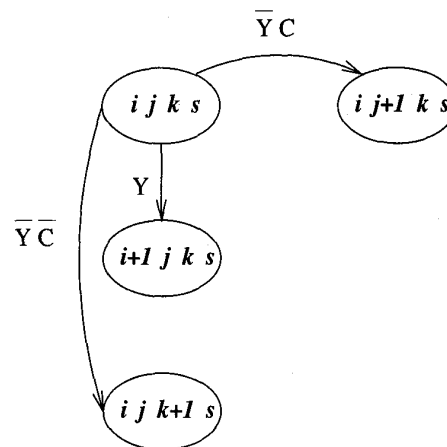


Figure 2. The state transition probabilities when the current chip is sampled for testing

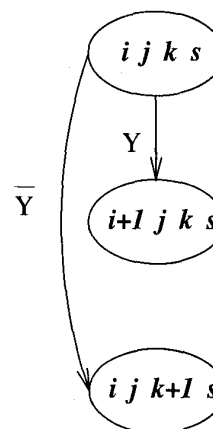


Figure 3. The state transition probabilities when the current chip is not sampled for testing

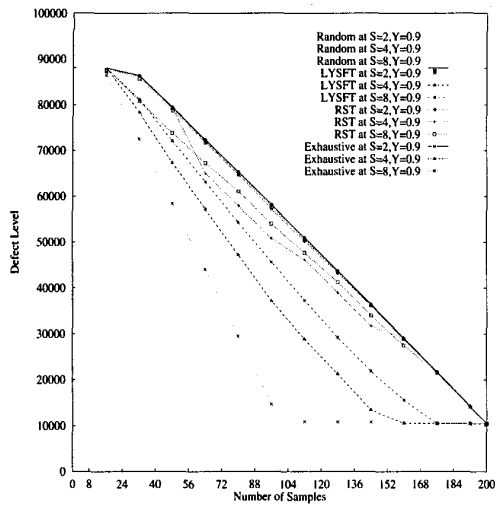


Figure 4. Defect level analysis for MCMs with KGY=90%

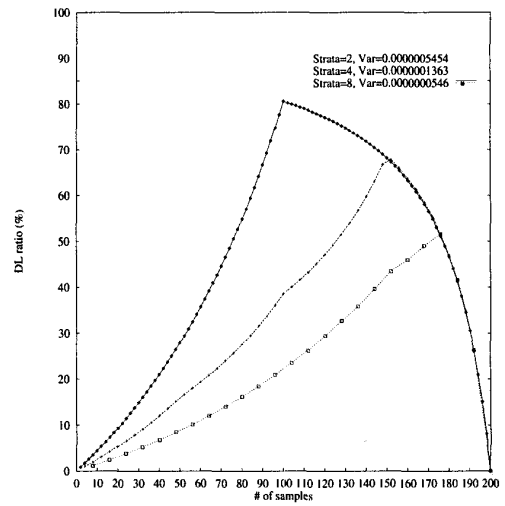


Figure 6. DL ratio (RT vs. LYSFT) by Stratified testing (at MCM Yield=90%,FC=90%)

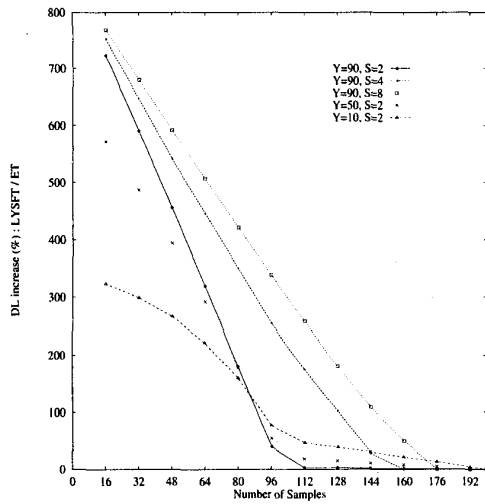


Figure 5. DL increase : LYSFT vs ET

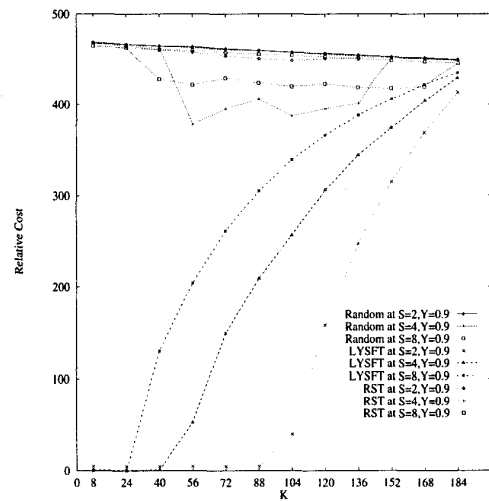


Figure 7. Cost analysis for MCMs with KGY=90%