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Quality Enhancement of Reconfigurable Multichip Module Systems by Redundant Utilization

M. Choi and N. Park
Department of Computer Science
Oklahoma State University, Stillwater, OK 74078-1053
{choim,npark}@a.cs.okstate.edu

F. Lombardi
Department of Electrical and Computer Engineering
Northeastern University, Boston, MA 02115
lombardi@ece.neu.edu

V. Piuri
Electronics and Information
Politecnico di Milano, piazza L. da Vinci 32, 20133 Milano, Italy
piuri@elet.polimi.it

Abstract – This paper evaluates the quality-effectiveness of the utilization of redundancy in reconfigurable MCM *(RMCM) systems. Due to the reconfigurability, a RMCM system can implement a device with different redundancy. Redundancy is determined by the requirement of the fault-tolerance (FT) of the device under implementation which is achieved by the feature of reconfigurability. No previous work has shown the effect of utilization of redundancy on quality-level (QL). In this paper, the tolerance to escaping from testing is introduced and referred to as the* escape tolerance *(ET). This can be achieved by utilizing a certain amount of redundancy and is studied by evaluating its effect on QL of RMCM under different amount of redundancy. Also, it is shown that the coverage of testing (FC) is improved by reconfiguration through numerical analysis. Hence, we derive the QL by relating the QL to the yield enhancement by reconfiguration; the effect of interconnection yield; the effect of ET to the QL; and the improvement in FC by reconfiguration. In the proposed approaches, appropriate combinatorial models are formulated to take into account parameters related to the redundancy and reconfiguration processes in RMCM systems. From extensive parametric results, it is shown that there exists a bound in the effectiveness of redundant utilization (i.e. the amount of redundancy) depending on the value of the RMCM yield and FC. Using the proposed approaches, redundant utilization of RMCM systems can be appropriately used to enhance the QL.*

Keywords – Field-Programmable-System, Multichip-Module, Quality Assurance, Utilization, Fault-Tolerance, Escape-Tolerance, Reconfiguration, Interconnection Yield

I. INTRODUCTION

The field programming systems (FPS) using FPGA and FPLD technologies are recently emerging as a quick-turnaround alternative to mask-programmed gate arrays of up to a few-thousand gates with a basic idea of replacing the metal interconnect which determines the personality of the gate array with SRAM-controlled pass-gates that could be programmed in the field instead of in the factory [2]. Although significant gains have been made in FPLD architecture and in the processing used to manufacture FPGA, the fact that FPLD are multipurpose requires the existence of a few resources on the FPLD that are underutilized in many applications, thus FPLD can provide flexibility that makes them useful, but also takes up valuable resources and adds to signal delays resulting in being less dense and slower than the same generation of ASIC, and the FPLD providers will always be challenged to find ways of making more powerful FPLD [2]. A new way to reduce risk and time in system-level development, while retaining a high level of logic integration, lies in the use of FPGAs [5]. The use of FPGAs provides benefits during all the stages of system development [5]. During prototyping the devices provide working hardware rapidly without the cost and delay of wire-wrapped standard device technology whether for a prototype or emulation of masked gate arrays [5]. However, FPSs combining large numbers of FPGAs are often bulky, expensive and slow, because the inherently low integration density of FPGAs forces a large part of the system interconnect to be carried in the upper levels of the packaging hierarchy, such as printed circuit boards (PCBs) and back-planes, rather than in the more cost effective integrated circuit technology [4].

MCM technology has the potential to revolutionize computing [4] as it can reduce the cost and increase the utility of FPS and dramatically increase the capability of FPLD and FPS in such a way that it can cost-effectively deliver 4-8 times the capacity of the largest FPLDs and provide even larger reductions in the area of PCB-based FPSs [2]. The design and special advan-

tages of the field programmable MCM (FPMCM) have been presented in [2].

Due to the inherent natures of MCMs, the achievement of an acceptable assembly yield and the requirement of product quality of the RMCM should also be assured [11]. There have been a few works on assuring the quality level (QL) of MCMs under various features such as uneven fault-coverage and imperfect diagnosis [11], repair process [12] and uneven known-good-yield [13]. Different implementations of a device reconfigurable on the RMCM have different qualities, which cannot be effectively evaluated by using previous approaches [11], [12], [13]. Hence, a new approach should be adopted to assure the QL of RMCM to take into account the effect of reconfiguration by using redundancy on the QL.

The objective of this paper is to evaluate the quality-effectiveness of the utilization of redundancy in RMCM systems by developing a quality model which takes into account the effect of fault tolerance and reconfiguration processes on the QL , and thereby to achieve the RMCM structure and testing strategies for the quality enhancement.

II. REVIEW AND PRELIMINARIES

For MCM, the effects of uneven fault-coverage and imperfect diagnosis on the QL have been shown in [11] and the repair process has been considered in evaluating the QL of MCMs in [12]. In [13], an uneven known-good-yield has been stressed and a novel stratified testing approach has been proposed for improving the QL of the MCM. There have been a few works on evaluating the QL but the effect of the reconfigurability on the QL has not been well considered and no consideration has given on the effect of redundant utilization of the chips and reconfiguration strategies. An example of a structure of a RMCM is shown in Figure (1) and the assumptions in this paper are as follows :

1. The RMCM is composed of multiple (N) identical FPGAs, whose known-good-yields and fault-coverages are even (identical).
2. Full interconnection structure is assumed as a criterion with the maximum overhead in interconnection testing.
3. Yield of each inter-chip interconnection is equal.
4. Testing is performed during the assembly phase [11].
5. Failure independence is assumed for the chips.
6. Selection of chips for reconfiguration of the RMCM is random.
7. No loss in yield due to reconfiguration process is assumed.

Factors and features (which appear in the next sections) are described as follows.

- N : number of chips on RMCM.
- Q : number of quorum chips.
- (i,j,k) : state in which i good chips, j bad chips and k escaped chips and $i+j+k \leq N$ during testing.
- (G,B,E) : state in which G good chips, B bad chips and E escaped chips and $G+B+E=N$ after testing completed and before reconfiguration applied.
- (g,b,e) : state in which g good chips, b bad chips and e escaped chips and $g \leq G$, $b \leq B$ and $e \leq E$ after testing and reconfiguration completed.

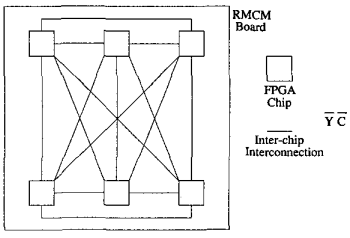


Fig. 1. An example of a fully connected structure of a RMCM

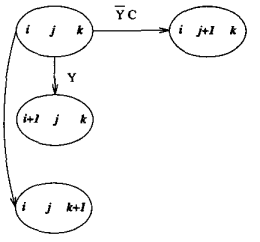


Fig. 2. States and transitions under imperfect fault-coverage

- Y_M : yield of a RMCM which takes into account both chips and interconnections.
- Y_m : yield of a RMCM which takes into account only chips without reconfiguration.
- Y_r : yield of a RMCM which takes into account only chips with reconfiguration.
- Y : yield of individual chip.
- C : FC of individual chip.
- Y_{int} : overall yield of interconnections.
- y_{int} : yield of each interconnection between each pair of chips.
- $CQL(N)$: QL of a RMCM with N chips without reconfiguration.
- $FRP(g,b,e)$ (*Field-Reconfiguration-Probability*) : the probability to be reconfigured in field with g chips out of G good chips, b chips out of B bad chips and e chips out of E escaped chips.
- $FET(G,B,E)$ (*Filed-Escape-Tolerability*) : probability for a state (G,B,E) to be escape-free (i.e. no escaped chip) in field after reconfiguration.
- $FQL(N,Q)$: probability for a RMCM (with Q chips of quorum out of N chips) to be escape-free.
- T_c : FC without reconfiguration.
- T_f : FC with reconfiguration.
- α : enhancement rate in FC due to reconfiguration.

III. REDUNDANT UTILIZATION FOR QUALITY ENHANCEMENT

Reconfiguration through redundant FPGAs is employed in conventional reconfigurable systems for the purpose of FT. Hence, the RMCM system performs reconfiguration to tolerate faulty FPGAs by utilizing redundant FPGAs and the effect of FT on the overall yield depends on the amount of redundancy. The yield enhancement through FT in reconfigurable gate arrays has been reported in a few works [6], [7] and can be extended to multiple FPGA systems. However, the QL, i.e. the yield of the system relating to confidence level of testing process or FC, of reconfigurable systems utilizing redundancy has not been reported. During reconfiguration in a reconfigurable system, not only can bad chips be tolerated but escaped chips can also be tolerated. Supposing there are g good, b bad and e escaped chips after testing the RMCM, ET is achieved by configuring the system of quorum Q only with good and bad chips excluding all the escaped chips if $Q \leq g+b$. Hence, assuming random reconfiguration of the system, the probability to configure the system satisfying this condition affects the QL of the system. Note that FT is achieved by configuring the system of quorum Q only with good and escaped chips excluding all the bad chips if $Q \leq g+e$. Thus, the overall QL can be formulated as a function of the effect of the reconfiguration on

FT, FC and ET, which is dependent on the utilization because the QL is well known as a function of yield (which is related to FT) and FC (which is related to ET) [8]. Traditionally, DL is defined [10] by

$$DL = 1 - Y_m^{1-C} = 1 - QL, \tag{1}$$

where Y_m does not assume any reconfiguration process (i.e. $Y_m = Y^N$). The yield of the RMCM with reconfiguration process (i.e. Y_r) is traditionally formulated as follows [9],

$$Y_r = \sum_{i=Q}^{N} \binom{N}{i} Y^i (1-Y)^{N-i}. \tag{2}$$

Since Equation (1) does not assume reconfiguration process, Y_m cannot be readily substituted with Y_r in Equation (2). Also, assuming fully connected structure of FPGAs in a RMCM as the worst case, the Y_{int} can be formulated by $Y_{int} = \sum_{i=1}^{N} y_{int}^{\frac{i(i-1)}{2}}$. Hence, Y_M of RMCM can be derived by $Y_M = Y_r \times Y_{int}$.

IV. ANALYSIS

As the testing and mounting processes of each chip are characterized stochastically, then it is possible to define a state of the system in which there are i tested-mounted-as-good chips (believed to be fault free), j tested-mounted-as-bad chips and k tested-mounted-as-escaped chips (passed the test process as good, while indeed bad) by vertex (i,j,k). At each state of this Markov model, there is only one untested chip for $N > i+j+k$, where N is the number of chips to be mounted on the substrate of the MCM. The quality level of MCMs is affected by the probability of the states in which $i+j+k = N$ and $k > 0$. The value of k is obviously a function of the fault-coverage and the diagnosability.

State transitions take place every time a chip is tested to be mounted. It is assumed that chips are selected for testing and mounted in an arbitrary order and the tests are independent (as in random testing). The state transition rates for every state under imperfect fault-coverage and perfect-diagnosis are shown in Figure (2). Figure (6) shows the state transition diagram of RMCM under imperfect fault-coverage and perfect diagnosis prior to reconfiguration, which is referred to as $CQL(N)$ where N is total number of FPGAs on the RMCM. From each state (i,j,k), $(N > i+j+k)$, three cases can occur (note that as no intermediate test and rework processes are assumed, there is no transition to $(i-1,j+1,k)$, $(i+1,j-1,k)$, $(i+1,j,k-1)$, $(i,j+1,k-1)$).

1. A just-mounted chip is tested, mounted and diagnosed as good, thus driving the system into state $(i+1,j,k)$ with probability Y.
2. A just-mounted chip is tested and diagnosed as bad, thus driving the system into state $(i,j+1,k)$ with probability $\overline{Y}C$. The implication of this transition probability is that a chip is correctly tested as bad only if the testing process detects all faults with a fault-coverage given by C.
3. A faulty chip is tested, mounted and diagnosed as good, thus driving the system into state $(i,j,k+1)$ with probability $\overline{Y}\ \overline{C}$. This implies that a chip can be faulty with probability $\overline{Y}$ and the testing process fails in detecting all faults with probability $\overline{C}$.

The overall $CQL(N)$ of a RMCM can be derived as a function of the known-good-yield (Y) and the FC as :

$$CQL(N) = \sum_{i+j=N} P(i,j,0) - P(0,N,0). \tag{3}$$

where the term $\sum_{i+j=N} P(i,j,0) - P(0,N,0)$ corresponds to the sum of the probabilities of the states in which there is no chip in an escape state after all the N chips have been tested and mounted (note that $P(0,N,0)$ is the probability of a state in which all the N chips have been tested and mounted as bad, i.e., no good and escaped chips). At each state (G,B,E) in Figure (6), where $G+B+E = N$, N = *total number of FPGAs on the system*, the FPGAs are supposed to undergo reconfiguration with a given Q. $FRP(g,b,e)$ is as follows.

$$FRP(g,b,e) = \frac{\binom{G}{g}\binom{B}{b}\binom{E}{e}}{\binom{N}{Q}} \tag{4}$$

Then, $FET(G,B,E)$ can be derived as follows.

$$FET(G,B,E) = \sum_{e=0} FRP(g,b,e),$$
$$0 \le g \le G, 0 \le b \le B, g+b = Q. \tag{5}$$

Hence, $FQL(N,Q)$ can be derived as follows.

$$FQL(N,Q) = \sum FET(G,B,E),$$
$$0 \le G \le N, 0 \le B \le N,$$
$$0 \le E \le N \text{ and } G+B+E = N. \tag{6}$$

However, as mentioned in the previous section, $FQL(N,Q)$ cannot readily relate the yield enhancement due to FT and the effect of reconfiguration on the FC, thus, the following steps are proposed. The $CQL(N)$ follows the conventional QL model [8] as follows,

$$CQL(N) = Y_m^{1-T_c}, \tag{7}$$

which holds because neither $CQL(N)$ and T_c is related to reconfiguration process. Thus,

$$T_c = 1 - log_{Y_m} CQL(N). \quad (8)$$

The effect of reconfiguration on the FC due to reconfiguration is considered in this paper. In RMCM as a user-programmable MCM, thorough testing of completed substrates, done as a byproduct of the programming process [1] since with only one test setup, each wire on the substrate is automatically pretested for shorts, and tested again after programming for opens, shorts, and electrical parameters. Hence, by the same tests, more faults can be covered in reconfigurable systems than in non-reconfigurable systems equipped with the same logic components. This feature is shown through numerical analysis in the following.

By employing the reconfiguration process on the same RMCM, the overall FC (T_f) can be formulated as

$$T_f = T_c + (1 - T_c)\alpha. \quad (9)$$

Now, the $FQL(N,Q)$ can be related to Y_m and T_f by following convention as

$$FQL(N,Q) = Y_m^{1-T_f}, \quad (10)$$

which holds because $FQL(N,Q)$ is not related to yield enhancement by FT (i.e. not related to Y_r). Hence, the enhanced value of FC for a the value of the raw yield of RMCM (i.e. Y_m) can be attained from Equation (10).

Hence, the value of α can be derived as follows by substituting T_f with $T_c + (1 - T_c)\alpha$ and T_c with $1 - log_{Y_m} CQL(N)$.

$$\alpha = 1 - \frac{logFQL(N,Q)}{logCQL(N)}. \quad (11)$$

It is shown in Figure(4) that using Equation (11) α increases as the amount of redundancy increases, thus the reconfiguration process improves the coverage of testing (i.e. FC).

Now, by following the conventional QL model [8] the resultant QL incorporating the effect of the yield enhancement due to FT and FC enhancement due to reconfiguration can be derived as follows.

$$QL = Y_M^{1-T_f}, \quad (12)$$

which holds because every term in the equation is related to reconfiguration features. In Appendix B, the analysis steps of the proposed approach is summarized.

Thus, the proposed QL model can effectively take into account the overall yield enhancement due to FT; the effect of reconfiguration on the overall FC; and the effect of ET on the overall QL.

V. PARAMETRIC ANALYSIS

The effect of redundant utilization on the QL in RMCM systems will be studied through numerical experiments in this section. Five kinds of theoretical RMCM systems with $Q = 1$, $Q = 2$, $Q = 4$, $Q = 8$ and $Q = 16$ will be investigated with $N = 16$ and $y_{int} = 0.9$ for each configuration. For the configuration 1, redundancy is given by 0 to 15 FPGA and 0 to 14, 0 to 12 and 0 to 8 for each configuration 2, 3 and 4, respectively; thus N=1 to 16, 2 to 16, 4 to 16 and 8 to 16, respectively. The QL of the configuration with Q=16 is shown in Figure (5) for the purpose of comparison. The effect of redundant utilization on QL has been researched under various sets of fault-coverage (C) on each FPGA, known-good-yield (Y_m) of the quorum of RMCM (i.e. $C = 0.1$ and 0.5 to 0.9 increased by 0.2 and $Y_m = 0.1$ and 0.5 to 0.9 increased by 0.2) and size N (note that redundancy is $N - Q$) for a given value of Q. The known-good-yield of each FPGA is calculated by $Y_m^{\frac{1}{Q}}$ and then the addition of $N - Q$ ($N > Q$) FPGAs will reduce the overall known-good-yield (i.e. Y_m of the RMCM by $\frac{Y_Q - Y_N}{Y_Q}$ (where Y_Q is Y_m and Y_N is $Y^{\frac{N}{Q}}$). The values of QL for given values of C are drawn in Figure (3(a))-(3(d)). By comparing the results, the followings can be observed.

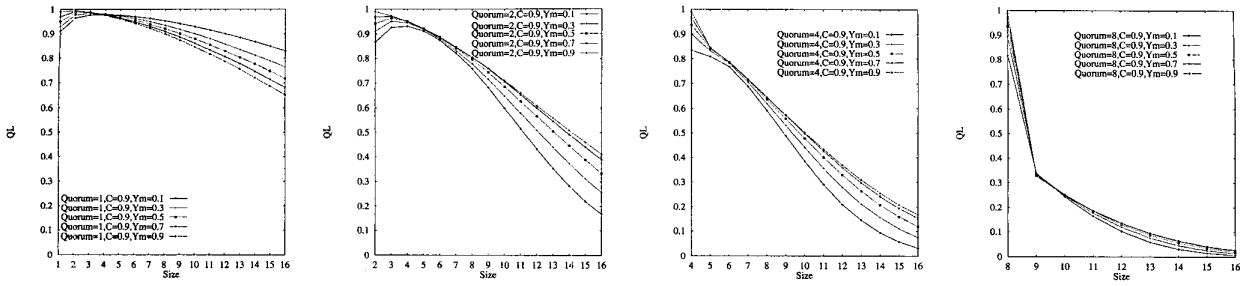
- The QL increases as the value of C increases at a given value of Y_m.
- The QL increases up to a certain value of size N but decreases after this value as Y_m increases at a given value of C. This value is formed at smaller size of N as C increases.
- The increase in the QL is bounded at a certain value of size N at given values of C and Y_m. This value is formed at larger size of N as Y_m decreases.
- Given the value of size N, the QL decreases as the value of Q increases.
- The value of size N at which the increase of the QL is bounded is smaller as the value of Q increases, and further the QL just decreases as the value of size N increases beyond a certain value of Y_m and Q.

Hence, from the above observations, the following conclusions can be drawn.

1. Given the values of Y_m, N and Q, redundant utilization enhances the QL better at high value of C.
2. Up to a certain amount of redundancy (or a certain value of N with a given Q), redundant utilization enhances the QL better for high yield systems but for low yield systems beyond that amount.
3. Low yield systems can use more redundancy to enhance the QL than high yield systems at a given value of C.

VI. DISCUSSION AND CONCLUSIONS

This paper has presented the evaluation of the quality-effectiveness of utilizing redundancy in testing RMCM sys-



(a) $Q = 1$ (b) $Q = 2$ (c) $Q = 4$ (d) $Q = 8$

Fig. 3. QL of RMCM at $Y_{int} = 0.9$

tems. Unlike previous methods [8], [9], [11], [12], [13], we have derived the QL by relating the QL to the yield enhancement by reconfiguration; the effect of ET to the QL; and the improvement in FC by reconfiguration. In the proposed approaches, combinatorial models are formulated to take into account parameters related to the redundancy and reconfiguration processes in RMCM systems based on the quality model proposed in [11].

From extensive parametric results it is shown that given the values of Y_m, N and Q, redundant utilization enhances the QL better; up to a certain amount of redundancy (or a certain value of N with a given Q), redundant utilization enhances the QL better for high yield systems but for low yield systems beyond that amount; low yield systems can use more redundancy to enhance the QL than high yield systems at a given value of C.

Hence, using the proposed approaches, a quality-effective redundant utilization of RMCM systems will be achieved; and thereby effective testing strategies and design-for-quality for RMCM systems can be ultimately achieved by exploring interconnection-for-quality.

Appendix A

After the $(i+j+k)$th chip is tested (and mounted) with an imperfect fault-coverage, the difference equations for the state diagram of Figure 6 are as follows:

$$P(i,0,0) = P(i-1,0,0)Y, \text{ for } j=0,\ k=0 \text{ and } i \geq 1 \quad (13)$$

$$P(0,j,0) = P(i,j-1,0)\overline{Y}C, \text{ for } i=0,\ k=0 \text{ and } j \geq 1 \quad (14)$$

$$P(i,j,0) = P(i-1,j,0)Y + P(i-1,j,0)\overline{Y}C, \text{ for } k=0 \text{ and } i,j \geq 1 \quad (15)$$

$$P(0,0,k) = P(i,j,k-1)\overline{Y}\,\overline{C}, \text{ for } i=0,\ j=0 \text{ and } 0<k<N \quad (16)$$

$$P(i,0,k) = P(i-1,0,k)Y + P(i,0,k-1)\overline{Y}\,\overline{C}, \text{ for } j=0,\ 0<k<N \text{ and } i \geq 1 \quad (17)$$

$$P(0,j,k) = P(0,j-1,k)\overline{Y}C + P(0,j,k-1)\overline{Y}\,\overline{C}, \text{ for } i=0,\ 0<k<N \text{ and } j \geq 1 \quad (18)$$

$$P(i,j,k) = P(i-1,j,k)Y + P(i,j-1,k)\overline{Y}C + P(i,j,k-1)\overline{Y}\,\overline{C}, \text{ for } 0<k<N \text{ and } i,j \geq 1 \quad (19)$$

$$P(0,0,N) = P(0,0,k-1)\overline{Y}\,\overline{C}, \text{ for } i=0,\ j=0 \text{ and } k=N, \quad (20)$$

where $P(i,j,k)$ represents the state probability of having i, j, k chips tested (and mounted) as good, bad, and escaped, respectively. Y and C represent the known-good-yield and the fault-coverage, respectively.

Appendix B

The following is the summary of the analysis steps of the proposed approach.

1. Calculate Y_M.
2. Derive the probability of each state (G,B,E) using Appendix A in Figure (6), where $G+B+E=N$.
3. Calculate each $FRP(g,b,e)$ by using Equation (4).
4. Calculate $FET(G,B,E)$ by using Equation (5).
5. Calculate α from the value of $FQL(Q,N)$ and by using equations (8)-(10).
6. Calculate T_f by using the value of α from step (5).
7. Derive the value of QL by using the values of Y_M from step (1) and T_f from step (6) as equation (12).
8. End of analysis.

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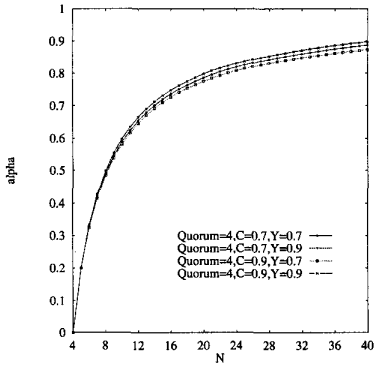

Fig. 4. Values of α at different C and Y

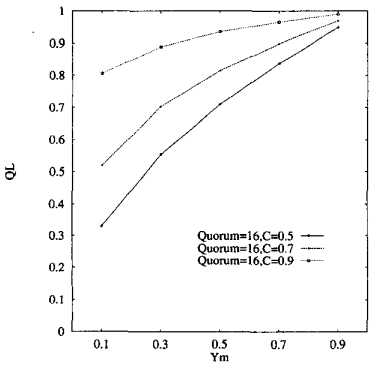

Fig. 5. QL of $Q = 16$ RMCM at $C = 0.5, 0.7, 0.9$ and $Y_{int} = 0.9$

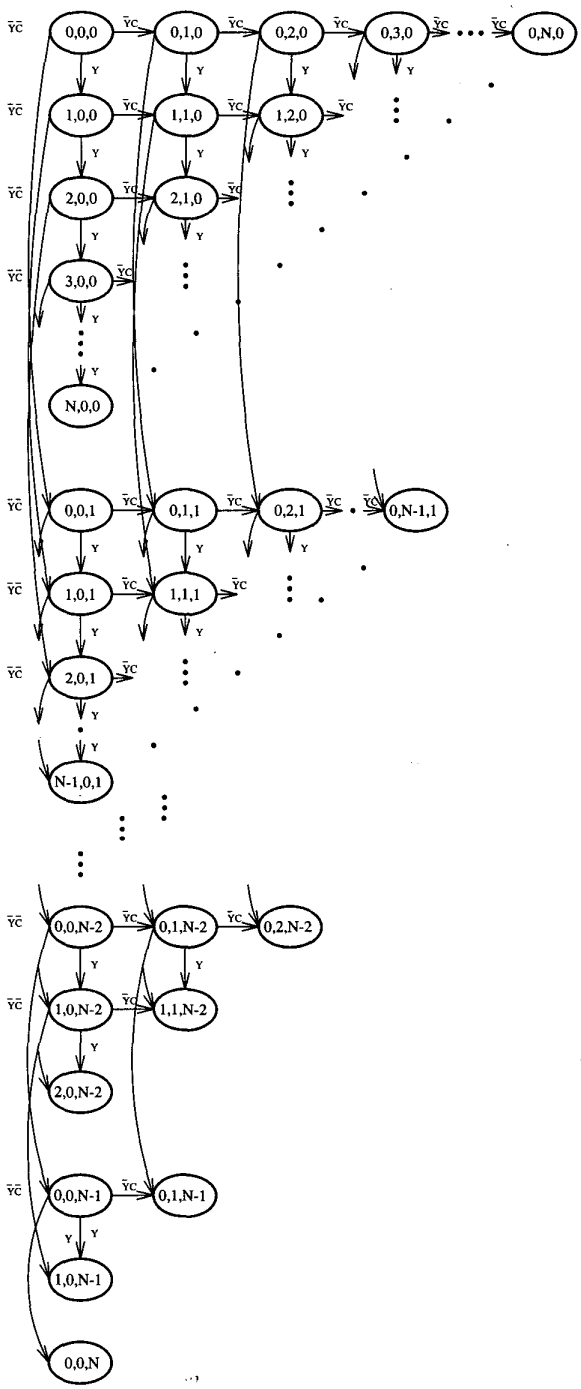

Fig. 6. CQL model