

Guest Editors' Column

Defect and fault tolerance are key issues for an effective realization of large, advanced integrated circuits and systems. Nowadays, they become particularly important for the increasing circuit complexity of modern systems, for the higher integration density of recent integration technologies, and for the hostile and safety-critical environments. All these characteristics are relevant for the growing diffusion of integrated circuits and systems in critical applications as well as in embedded systems, e.g., for automotive, avionics, nuclear systems, real-time process control systems, consumer electronics, instrumentation, and robotics. Feasibility and competitiveness are in fact strictly related to production yield, quality assessment by testability and testing, operating behavior correctness by concurrent checking, and system survival by reconfiguration.

Many efforts are therefore spent by researchers and practitioners in order to have better understanding of phenomena underlying defect and fault occurrence in VLSI systems, accurate models describing and predicting defect and fault occurrence and distributions, architectural solutions for yield enhancement and system survival, efficient and effective techniques and tools for testing, concurrent checking, correction, and diagnosis.

At the 1997 IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems, held in Paris, France, on October 20-22, 1997 some recent results related to the theory, the applications and the implementation technologies for defect and fault tolerance were presented. Close interaction and interdisciplinary nature of the knowledge background and expertise of the audience allowed for in-depth discussion of hot topics, confrontation of different techniques and sharing of experiences for further mutual stimulation between research and practical application of innovative ideas and solutions.

In this special issue, selected papers were reviewed and chosen to expand and discuss preliminary results presented by the authors at the symposium as well as to reach a wider audience. Selected papers cover most of the problems in defect and fault tolerance.

Reliability modeling is an important issue which allows to evaluate the effectiveness of detecting and reconfiguration techniques with respect to their costs in terms of redundancy, latency, throughput and, as a consequence,

economical impact. The problem of system modeling for reliability evaluation is afforded in *Are defect-tolerant multi-processors array with redundancy really cost-effective? Complete and realistic cost model* for a specific class of architectures, even if the approach can be extended to a wider spectrum of systems.

High yield and reliability can be also achieved by adopting avoidance techniques: an accurate and intelligent design of the integrated devices may lead to a quality increase. Suitable design strategies and CAD tools are required to support these approaches. In *Three-layer routing for more reliable design*, advanced VLSI design technique and tool are presented to enhance the reliability by avoiding electromagnetic effects within wiring.

Testing is another issue to identify the presence of defect at the end of production and to assess the quality of products. Due to the increasing complexity of the modern systems, testability and testing assume a relevant role in this view. In *Testing of Programmable Logic Devices (PLD) with faulty resources*, the case of a class of devices which are becoming of large use is discussed with an innovative approach. *Detecting bridging faults in CMOS domino logic via on chip dynamic power supply current monitor* affords the analysis of complex bridging defects in one of the widely adopted integration technologies.

Detection of the presence of errors due to life-time faults is another important issue to guarantee the quality of circuits and systems, their behavior, and the correctness of the outputs. *Design of encoders and self-testing checkers for some systematic unidirectional error detecting codes* provides the theoretical framework and some practical solutions to the design of self-checking systems for an important class of data coding technique. In *On-line self-testing voting scheme for TMR systems*, a strategy to implement self-checking voters and systems is presented with a limited redundancy overhead. *Data recovery and error identification in parallel data compaction* deals with the use of signature compression and analysis to detect and correct errors in very large systems with a limited number of observation points.

The growing complexity of the future circuits and systems as well as the novel integration technologies will require further research and practice for device and system modeling,

acquisition and monitoring of real process measurement and statistics, yield estimation, reliability evaluation, testing, testability evaluation, detection techniques, correction techniques, self-checking devices, system restructuring and reconfiguration, CAD tools for assisted design directed to enhance yield and reliability.

These will be the challenges of the near future to support the practical use of integrated circuits and systems in a increasingly wide spectrum of application, not only in advanced fields, but also in the daily life.

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