Testing and Evaluating the Quality-Level of Stratified Multichip Module Instrumentation

Nohpill Park, Fabrizio Lombardi, and Vincenzo Piuri

***Abstract*—In this paper, approaches to measuring the quality-level of multichip module (MCM) instrumentations are proposed. The MCM is generally composed of a number of sets (or strata) of chips with different known-good-yields (KGYs), so-called *stratified,* since each stratum is procured from a separate manufacturer. This characteristic of MCM is employed to enhance the performance of the testing process thereby assuring the quality-level of MCMs. A stratified technique is proposed for testing MCMs. Its advantages are an improvement in quality-level and cost-effectiveness. The proposed testing approach is accomplished in the presence of uneven KGY for MCMs consisting of different sets (or strata) of chips. This approach referred to as the lowest yield-stratum first-testing (LYSFT) considers the unevenness of KGY between strata for testing the chips and improving the QL. For comparison purposes, exhaustive testing (ET), random testing (RT), and random stratified testing (RST) are also evaluated by using a Markov-chain model.**

Given the strata, KGY and the sample size of the chips under test, the proposed LYSFT approach allocates and tests the sampled chips in a greedy (first) fashion, while RT and RST select the chip (for RT) and the stratum (for RST) randomly. A Markov-chain model is used to analyze the quality-levels of these testing approaches and is solved analytically in $O(SN^3)$ for the LYSFT (where S is the number of strata and N is the number of chips in the MCM). A cost model is proposed and shown as figure of merit and shown to relate the defect-level with the number of tests performed.

Parametric results show that the LYSFT dramatically outperforms RT and RST for improving the quality-level. A considerable reduction in tests can be achieved by the LYSFT at a very small loss in quality-level compared with ET. Based on the proposed cost model, it is also shown that the LYSFT is the most cost-effective strategy. The validity of the proposed approach is further proved through Monte Carlo simulation.

***Index Terms*—Instrumentation, multichip module, quality-level, stratification, testing.**

I. Introduction

MULTICHIP module (MCM) is a technology which provides high-density packaging by mounting chips directly onto a substrate [5]. The need for MCMs arises due to the inability of current technology to embed an entire complex system on either a single large chip, or a wafer using wafer-scale integration (WSI). Multichip module technology has been used to offer significant improvements in a number of instrumentation industries, including high energy physics instrumentation computing, spacecraft data system instrumentation, scientific instrumentation, automotive instrumentation, and instrumentations in consumer applications [1]–[4], [8], [7]. Its advantages are miniaturized size, reduced weight, high frequency operation, improved thermal performance, and improved reliability, to mention a few.

Some of the most challenging problems for MCMs are the achievement of an acceptable assembly yield and the requirement of product quality [25]. For VLSI manufacturing, products must be tested thoroughly to ensure correct fabrication [13]. A commonly used method for VLSI is random testing in which input test patterns are generated randomly [12], [13], [16], [17], [15], [14]. However, it is very costly (if not impossible) to exhaustively test VLSI chips for detecting all defects [13], especially for high-density systems such as MCMs. Thus, instead of an exhaustive process, these chips are tested using only a fraction of the exhaustive patterns at a cost of leaving some defective products undetected and shipped as good [13].

The growth experienced by MCMs has resulted in a very high chip count; random testing is fast becoming a realistic alternative for MCMs, too. MCM testing is complicated because the issue of known-good bare chips (due to separate procurement of the chips, for example) makes it difficult to guarantee that high quality can be fully maintained [10]. This results in a wide variation of known-good-yields (KGY) and in different fault-coverage (FC) [18] between chips too. In this paper, these features of MCMs are referred to as *uneven KGY* and *uneven FC* [18], respectively. Uneven FC in exhaustive testing (ET) has been studied in [18] for a reduction in quality level (QL) under even KGY between chips. Like [18], in this paper, testing coverage between chips is uneven as very stringent requirements must be met for chips with low KGY. *Exhaustive testing* (ET) [18], [5], [9], [25], [21], [20] and *random testing* (RT) are defined as the process which tests every chip, and the process which tests only a number of randomly sampled chips in the MCM, respectively (note that chip sampling is the process of selecting a chip for testing). Therefore, conventional exhaustive and random testing [12], [13], [16], [17] for a VLSI chip can be extended to the scenario of multiple chips as applicable to systems such as MCMs. Also, *random stratified testing* (RST) is introduced in this paper; RST is defined as the process which tests chips from randomly sampled sets of equal chips (or stratum) on the MCM first.

The MCM is generally composed of a number of sets (or strata) of chips with a different KGY; each stratum is procured from a separate manufacturer. Without loss of generality, the

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TABLE I
QUALITATIVE COMPARISON BETWEEN TESTING STRATEGIES FOR MCMs

Comparison	LYSFT	RT	RST	ET
QL	2	4	3	1
Test time	3	1	2	4
Test length	1	1	1	2

variance in KGY between chips in a stratum is usually *small*, while variance between strata can be *larger* than between chips in a stratum. In this paper, this is referred to as *stratification*. This characteristic of MCMs is employed to enhance the performance of RT and reduce the number of tests, thus, ultimately reducing the cost of testing each stratum based on its KGY value. This process is referred to as *stratified testing*, i.e., a testing process based on stratification. The overhead for chip sampling based on the KGY of each stratum is $O(S)$ (where S is the number of strata in the MCM), not $O(N)$ as in [18], as based on the KGY of each individual chip (where N is the number of chips on the MCM). Therefore, testing is accomplished by exploiting the homogeneity between chips in each stratum and the heterogeneity between strata.

The *unevenness* of FC in RT occurs between strata, i.e., different numbers of chips are sampled and tested in each stratum based on the KGY. Hence, a *lowest-yield-stratum first-testing* (LYSFT) approach is proposed and evaluated as the basic criterion for *stratified testing*. A qualitative comparison between testing strategies for MCMs is summarized in Table I. In Table I, each strategy is ranked as follows: 1 (4) stands for the strategy which achieves the highest (lowest) QL; the strategy which requires the shortest (longest) time; the strategy which utilizes the smallest (largest) number of tests.

The main objective of this paper is to demonstrate the feasibility of stratified testing (i.e., the LYSFT) for MCMs by evaluating the QL and cost reduction based on a cost-model under uneven KGY between strata. This is used to achieve cost-effective testing compared with RT and RST (for improving the QL) and ET (by reducing the number of tests at an acceptable small loss of QL).

The organization of this paper is as follows. In the following section, we review related work as well as introducing the preliminaries and the basic principles of the proposed approach. In Section III, the lowest yield stratum first testing (LYSFT) approach is introduced. Section IV describes the analytical approach for evaluating the LYSFT approach based on a novel Markov model. In Section V, a parametric analysis is provided to demonstrate and validate its accuracy and efficiency. In the final section, discussion and conclusions are presented.

II. REVIEW

Today's MCM testing general Today's MCM technology allows the design of systems so complex they are virtually impossible to test exhaustively due to an excessive time overhead and severe limitation in available electrical access. This severely restricts the use of conventional testing approaches [5]. These problems can be significantly alleviated by adopting novel approaches to guarantee the quality of incoming bare (unpackaged) chips prior to module assembly, the structural integrity and performance of the assembled MCMs, and to isolate defective parts prior to repair [25].

In [25], it has been shown that the above problems can be solved by adopting a structured testability approach. Design for testability (DFT) is expected to be one of the cost-effective solutions for structured MCM testing [5]. BIST and boundary scan are usually used to implement DFT [9], [22], [21]. Also, a variety of test and inspection techniques (such as optical inspection, proximity electrical testing and electron-beam testing) have been developed for PCBs, VLSI, and WSI, and can be used for MCMs, too [20]. The factors that determine the feasibility of an approach are the cost (and time) for performing the test, the provided fault coverage, and the extent to which subsequent faults are created due to damage in the substrate [20].

The effects of repair on the QL of MCMs using ET have been studied in [19] and a QL analysis model has been developed by relating the QL to the uneven FC and imperfect diagnosis [18]. Traditionally, the number of tests and test generation complexity are reduced by random testing (RT) [12], [14]–[17]. Extensive research has been performed on random testing of VLSI [12], [14]–[17]. This can be extended to MCMs by using a chip-level model, rather than a fault-level model. In this paper, it will be shown that RT provides an unacceptable large loss in QL by reducing the number of tests with no discrimination in sampling chips which will provide a significant number of escaped chips.

The reduction in hardware overhead has been studied in [23], [24]. In [23], it has been shown that a partial boundary scan can reduce the hardware overhead by 14%–50% compared with a full scan design, while still maintaining the same level of fault coverage. In [24], part selection criteria have been studied for partial testing. Unlike the approaches for reducing hardware overhead [23], [24], the proposed approach is motivated by the reduction in the complexity of test vectors, while maintaining the same amount of hardware overhead.

For MCM technology, discrete VLSI chips of different types are mounted on a wafer substrate (such as global power, clock, and distribution networks). An example of the MCM for hybrid-WSI is given in Fig. 1 [7]. In Fig. 1, the chips of the same type are assumed to constitute a *stratum* (i.e., there are 5 strata by definition of stratum in this paper). Chips of the same type are procured from the same manufacturer with a uniform KGY (i.e., a low variance in their KGY). A heterogeneity in KGY (i.e., high variance in KGY) between chips in different strata is assumed as different manufacturers can be involved. This is referred to as *stratification*.

III. PRELIMINARIES AND NOTATIONS

In this paper, a testing strategy is proposed based on the stratification of MCMs. In general [6], sampling based on strata (*stratified sampling*) reduces the variance of the estimate, provided each stratum is homogeneous and heterogeneity is applicable between strata. Unlike conventional stratified sampling,

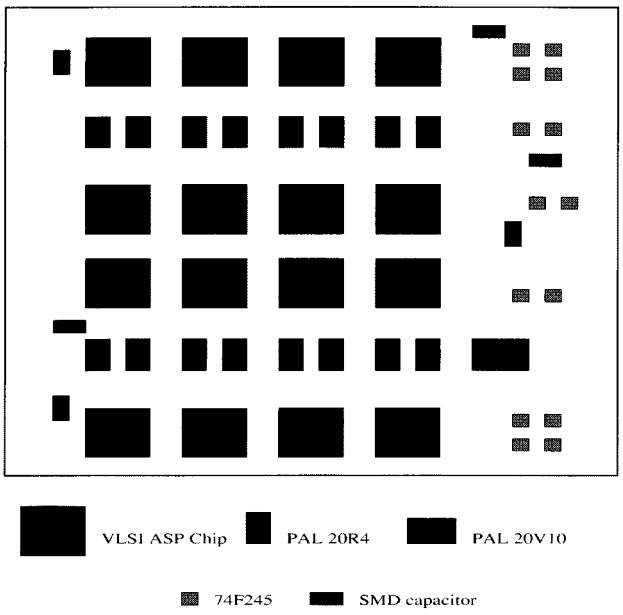

Fig. 1. MCM composed of discrete VLSI chips.

chip sampling in the proposed testing approach enhances the QL of the MCM. By stratifying the MCM, chips can be sampled for testing at a small complexity, i.e., $O(S)$ where S is the number of strata.

The main feature of stratification is to exploit the uneven KGY between strata. In stratified MCMs, the chips in the stratum with lower KGY are more likely to be faulty than the chips in the stratum with a higher KGY. This may result in failing to sample chips with lower KGY. This will also cause a significant degradation in the QL than sampling chips with higher KGY (provided RT is employed). Hence, by sampling chips based on stratification, testing on strata of different KGY can be performed, such that more chips are sampled from the stratum with lower KGY than from the stratum with higher KGY. Thus, the proposed approach can solve the complexity issues of RT (and its serious loss in QL) as well as the overhead of ET.

The notation used in this paper is as follows.

$LYSFT$	Lowest yield stratum first testing.
RT	Random MCM testing.
RST	Random stratified testing.
ET	Exhaustive MCM testing.
$QL(DL)$	Quality level (defect level).
Y, KGY, FC	Yield, known-good-yield, fault coverage.
N, N_S	Number of chips in the MCM, number of chips in a stratum.
S	Number of strata in the MCM.
SPL	Number of chips sampled from the MCM.
$sample(S)$	Number of chips sampled from stratum S.
$size(S)$	Number of chips in stratum S.

The assumptions for the Lowest Yield Stratum First Testing (LYSFT) are as follows:

1) Testing is performed during the assembly phase [18]; testing of each chip is performed using traditional VLSI techniques. Every chip on the MCM is assumed to be testable and a more comprehensive test method than production testing is available prior to assembling.
2) The MCM is assembled using unequal chips with different KGYs. System diagnosis is assumed to be perfect.
3) The hardware overhead of each testing strategy (i.e., exhaustive, RT and stratified testing) is not considered.
4) Failure independence is assumed for the chips. Interconnections and substrate yields are assumed to be perfect.
5) No repair process is utilized.
6) As the MCM is composed of a number of strata, each of which consists of a certain number of chips, then testing is performed stratum by stratum.

IV. Lowest-Yield-Stratum First-Testing (LYSFT)

For RT, the number of sampled chips in each stratum is commonly assumed to be even as no discrimination in the selection process is employed. A serious loss in QL could result by testing every chip with an even weight, i.e., excessive testing of high KGY chips and a lack of testing for low KGY chips may occur. Hence, the LYSFT is proposed for selection in testing a stratum.

In the proposed LYSFT, given the number of tests and hardware overhead, testing of the chips is based on the KGY of the stratum. LYSFT is a very straightforward approach that greedy (first) allocates and samples chips from the stratum with the lowest KGY. Thereby, the chips in the stratum with the highest KGY are selected last for testing. The main characteristics of this approach are as follows:

1) The time overhead for stratifying chips in the given MCM is negligible [i.e., $O(S)$, where S is the number of strata].
2) Due to the separate procurement of chips in MCMs, variance of the KGY is assumed to be small in a stratum and large between strata[6].
3) For nonsampled chips, the probability to escape in testing is given by the probability to be bad (i.e., $1-Y$, as Y is the KGY of a chip). Hence, the impact of escaping on the QL for chips with a low KGY can be significant. The main objective of the LYSFT is to reduce the overall probability of escaping for low KGY chips by testing low KGY chips greedy (first).

Given Y, C, and S, the proposed approach consists of the following chip-level steps.

1) A good chip is tested as good, with probability Y.
2) A bad chip is tested correctly as bad, with probability $\overline{Y}C$.
3) A bad chip is tested incorrectly as escaped, with probability $\overline{Y}\ \overline{C}$.
4) All the bad chips not selected for testing escape, with probability $\overline{Y}$ and all the good chips not selected for testing do not affect the QL.

As shown in previous work [18], testing, and mounting during assembly are stochastic processes. Also, the random chip selection process within a stratum and testing on a stratum-by-stratum basis (in an arbitrary order) are stochastic. Hence, a Markov based model can be appropriately formulated for analyzing the QL of the LYSFT. Using the proposed Markov model, it is possible to evaluate the effect of the LYSFT on the QL

during assembly. One of the objectives of this paper is, therefore, to find an effective partial testing strategy for MCMs under uneven KGY between strata [6].

V. Analysis of the LYSFT

In the proposed Markov model, a state (i, j, k, s) for the stochastic processes of testing and mounting each chip is defined as follows: i out of N_s chips in stratum s (where N_s is the number of chips in stratum s and s is the stratum currently under test) are tested-mounted-as-good, j out of N_s chips in stratum s are tested-mounted-as-bad and k chips out of $\sum_{c=1}^{s-1} N_c + i + j + k$ are tested-mounted-as-escaped up to $s-1$ strata and up to the current chip in stratum s under testing. Note that the value of k is cumulative throughout the whole strata, thereby excluding all the states with chips escaped in the testing process.

At each state, there is only one untested chip for $N_s > i+j+k$ and $S \geq s$ (where S is the number of strata in the MCM). The defect level (DL) of the MCM is given by the sum of the probabilities of the states in which $i + j + k = N$, $k > 0$ and $s = S$. The value of k is obviously a function of both the KGY and FC (under the assumption of perfect diagnosis and no repair).

State transitions take place every time a chip is tested and mounted. Tests are independent for RT, commonly by using an appropriate hardware arrangement [25]. The state transition rates for every state when the current chip is selected (sampled or not) for testing, are given in Figs. 2 and 3, respectively.

From state (i, j, k, s), ($N > i + j + k$ and $S \geq s$) in Fig. 2, three transitions can occur and are defined as follows:

1) A just-mounted chip is tested, mounted as good, thus driving the system into state $(i+1, j, k, s)$, with probability Y.
2) A just-mounted chip is tested as bad, thus driving the system into state $(i, j+1, k, s)$, with probability $\overline{Y}C$. The implication of this transition probability is that a chip is correctly tested as bad only if the testing process detects all faults with probability C.
3) A faulty chip is tested, mounted as good, thus driving the system into state $(i, j, k+1, s)$, with probability $\overline{Y}\,\overline{C}$. This implies that a chip can be faulty, with probability $\overline{Y}$ and the testing process fails in detecting all faults, with probability $\overline{C}$.

From state (i, j, k, s), ($N > i + j + k$ and $S \geq s$) in Fig. 3, two transitions can occur and are defined as follows:

1) A just-mounted good chip is not tested and mounted (as good), with probability Y.
2) A just-mounted bad chip is not tested, but mounted (as good), with probability $\overline{Y}$.

Note that after RT of a stratum, the state transitions from each state (i, j, k, s) (where $s < S$) flow into the next three states: $(1, 0, 0, s+1)$, $(0, 1, 0, s+1)$ and $(0, 0, 1, s+1)$. So, the states with $k > 0$ are effectively excluded from the states with $k = 0$, to simplify the calculation of QL.

All probabilities $P(i, j, k, s)$ for every state (i, j, k, s) can be calculated from the equations in the Appendix. Therefore, the overall QL and DL of the MCM using the LYSFT can be derived as a function of the KGY (Y), the FC (C) and the number of

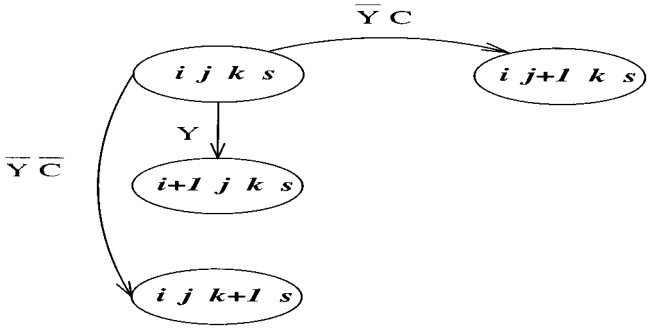

Fig. 2. State transition probabilities when the current chip is sampled for testing.

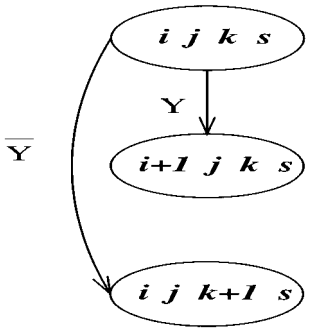

Fig. 3. State transition probabilities when the current chip is not sampled for testing.

chips and sampled chips in each stratum. These are given as follows

$$QL = \sum_{i+j=N,\, j \leq t_S} P(i, j, 0, S), \tag{1}$$

$$DL = 1 - \sum_{i+j=N,\, j \leq t_S} P(i, j, 0, S) = 1 - QL \tag{2}$$

where S is the number of the last stratum tested and t_S is the number of samples for the last stratum. The time complexity (T) of this algorithm is $O(SN^3)$. The proof is as follows

$$T = \sum_{s=1}^{S} \sum_{k=0}^{N} \sum_{j=0}^{sample(s)} \sum_{i=0}^{size(s)} K$$

where K is the number of computational steps in the innermost loop in the algorithm [a constant equal to $O(1)$]. The worst case sizes of $sample(s)$ and $size(s)$ are both N, hence the overall time complexity of $Calc\_DL\_LYSFT$ is given by $O(SN^3)$ as stated previously.

Based on the model and the algorithm proposed, the DL of RT can also be calculated by evenly allocating sampled chips for every stratum instead of allocating according to the lowest yield stratum first.

The QL of RST can be evaluated based on the proposed model as follows

$$QL = \sum_{i=1}^{sset} \frac{1}{sset}\, ql_i \tag{3}$$

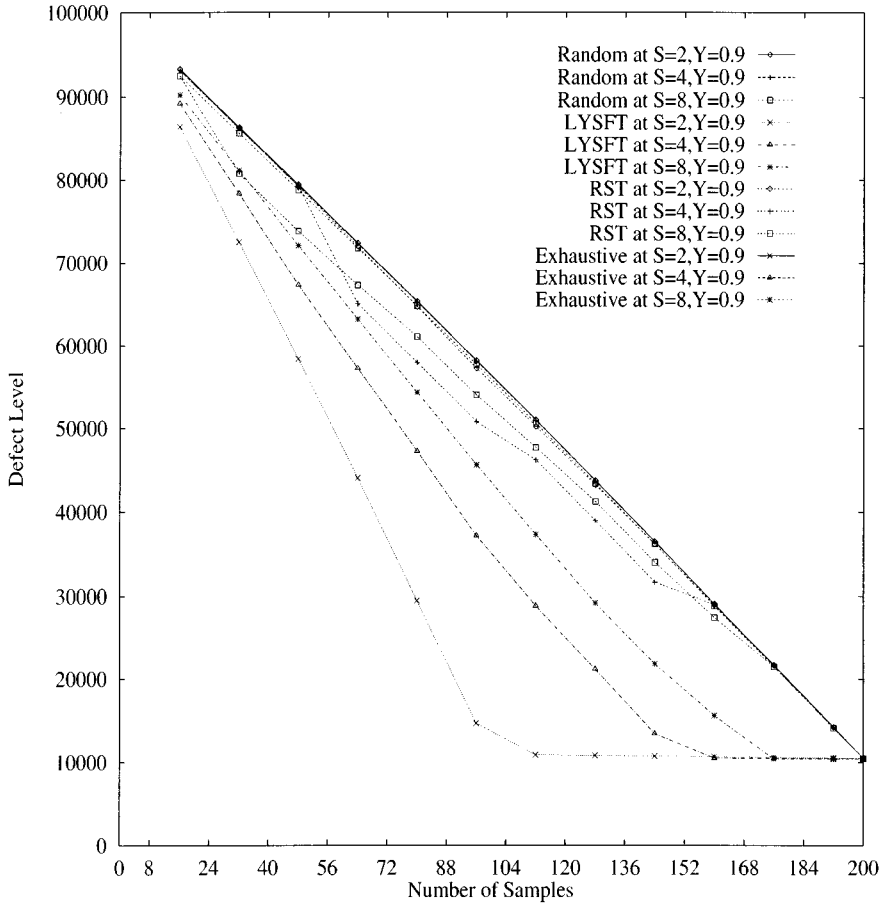

Fig. 4. Defect level analysis for MCMs with KGY $= 90\%$.

where $sset$ is the number of all the possible sets of stratum sampling. This is given by ${}_SC_rR$ where r is the quotient of $SPL/ssize$, ${}_SC_r = S!/(r!(S-r)!)$, and SPL and $ssize$ are the number of total chips and the number of chips in each stratum to be sampled (note that in this paper $ssize$ is assumed to be the same for each stratum), respectively. R is the number of all the possible combinations for allocating samples to the last stratum (i.e., less than the whole stratum can be allocated for the last sampled stratum). Due to randomness, the probability for each stratum to be sampled is $1/sset$. ql_i is the QL of the chips sampled for the ith combination and is given by using the same model with the LYSFT and $Calc\_DL\_LYSFT$.

The overall DL of the ET with uneven KGY is calculated using the same Markov-model and the same algorithm of [18] with a fixed value for the FC.

VI. Parametric/Cost Analysis

In this section, the effect of the LYSFT on the DL of MCMs will be studied through numerical experiments and its performance will be compared with RT, RST, and ET.

The yield of the MCM is calculated as a series product of the KGYs (Y) of all chips. This shows a variance between the average KGY of the strata. In this paper, the FC is given by 0.9 for every chip in each test, independent of the testing process (i.e., for LYSFT, RT, RST, and ET). The number of chips on the MCM is given by 200 and the number of strata on the MCM is given by 2, 4, 8. Due to the random chip selection in the LYSFT, RT and RST, the KGY of each chip is given by the average KGY of the chips in its stratum. As the number of strata increases, then the variance (Var) between average KGYs between strata also decreases. The variance decreases as the MCM yield increases.

As mentioned earlier in a previous section, the DL of each test strategy (i.e., the LYSFT, RT, RST, ET) is calculated under an uneven KGY. In Fig. 4, the DL of each strategy is plotted versus number of samples and variance of KGY between strata (for a given value of KGY of the MCM). Note that the convergence in Fig. 4 shows the DL of ET.

By analyzing the results of Fig. 4, the following features are observed.

- The DL of the LYSFT decreases as the Var, the MCM yield and the number of samples are increased, i.e., the performance of the LYSFT is better at high MCM yield and at high Var for a large number of samples.
- The DL of the RT decreases as the MCM yield increases and is only slightly affected by Var. By comparing the DL of the RT with the DL of the LYSFT, it is observed that the DL of the RT is higher than for the LYSFT independent of Var, MCM yield and the number of samples.
- The value of the DL of RST is between the DLs of the LYSFT and the RT, for a given Var and MCM yield.

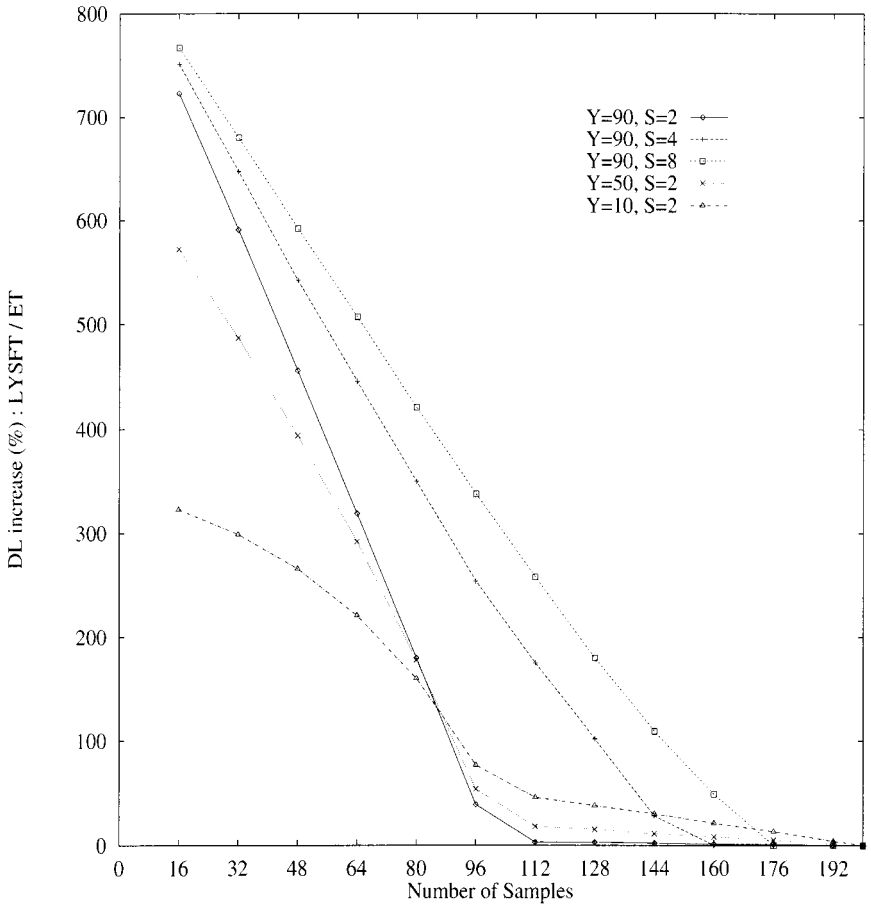

Fig. 5. DL increase: LYSFT versus ET.

- By comparing the DL of the ET to the LYSFT, it is shown that the DL of the LYSFT is competitive with the DL of the ET with a considerable reduction in the sample size at high MCM yield and Var, i.e., the LYSFT at sample size of 120 and $S = 2$ ($\mathrm{Var} = 0.5454 \times 10^{-6}$) in Fig. 4.

The DL increase of the LYSFT is plotted in Fig. 5. The following observations can be drawn.

- For example, the DL increase for the LYSFT is very small [i.e., a 3(%) for 112 sampled chips out of 200 and the MCM yield of 0.9 and $S = 2$ (i.e., $\mathrm{Var} = 0.5454 \times 10^{-6}$)].
- An acceptable sample size is shown at different Var for the MCM yield $= 0.9$. This acceptable sample size level is lower at high values of Var.

To evaluate the DL ratio (%) (i.e., DL_{RT}/DL_{LYSFT}) of the RT compared to the LYSFT, its increase is plotted in Fig. 7 over the whole range of sample sizes.

- The DL ratio increases as the MCM yield increases.
- Given the number of strata and the size of each stratum, there exists a value of sampled chips for a minimal DL increase, i.e., 100 when $S = 2$, 152 when $S = 4$ and 176 when $S = 8$.
- At high MCM yield (i.e., >0.9), the DL increase for the high Var value case (i.e., $S = 2$ in each Figure) is always higher than for lower Var value cases. As the MCM yield decreases, the DL increase for the medium Var case (i.e., $S = 4$ case) becomes higher than for the high Var case.

However, the DL (or QL) is not fully representative as a sole figure of merit for testings MCMs during assembly phase. Hence, a new cost model as figure of merit is introduced to relate the cost to the DL and the number of chips to test. This is given as follows:

$$Relative\_Cost(K) = \frac{DL_i - DL_{exh}}{K}, \quad \text{for } K = N_{exh} - N_i \tag{4}$$

where DL_i and DL_{exh} are the DL of the ith testing strategy and ET, respectively, and N_i and N_{exh} are the number of chips tested by the ith testing strategy and ET, respectively. Thus, it is referred to as the $Relative\_Cost$, i.e., the cost relative to the DL and the number of tests for the ET.

Expression (4) can be explained as follows: ET delivers the highest quality MCM. However, this does not imply that a long test time is really required for all cases. An excessive amount of testing may not necessarily result in a profitable final MCM and a long test may impact the costs of the final MCM, i.e., costs for testing resources and manufacturing throughput (MCM units manufactured per unit time) are directly affected. Hence, by taking into account a reduction in the number of chips to test and the DL increase (relative to ET), $Relative\_Cost$ calculates the actual profit of each testing strategy.

The cost of each strategy is shown in Fig. 6 based on $Relative\_Cost$ in equation (4).

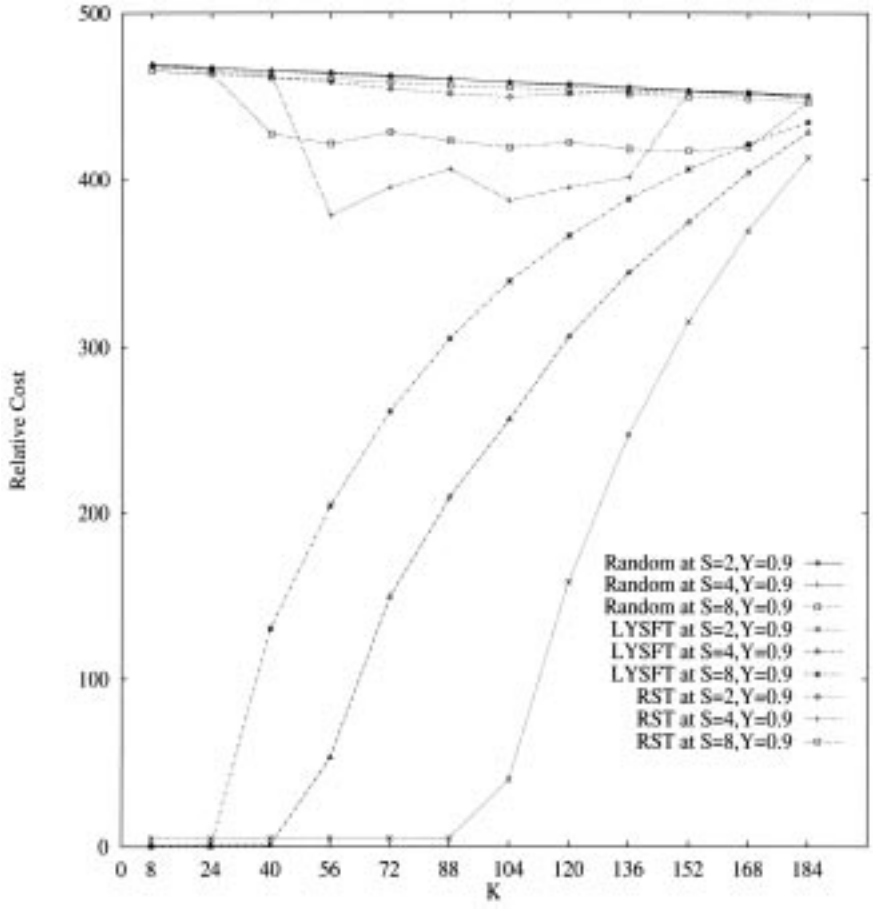

Fig. 6. Cost analysis for MCMs with KGY = 90%.

From the results of Fig. 6, the followings observations can be drawn.

- For the entire range of values of MCM yield, Var and sample size, the LYSFT always outperforms the RT and the RST in cost.
- The relative cost of the LYSFT increases as the value of K increases (i.e., the number of samples decreases). However, for a large value of K and a small value of MCM yield, the relative cost of the LYSFT decreases.
- With a small number of samples, the LYSFT performs better in cost at low values of Var (i.e., it has a small cost).
- Beyond a certain large number of samples (i.e., about 40 in Fig. 6), the LYSFT performs better in cost at high values of Var.
- Given a sample size and MCM yield, the LYSFT performs better at high values of Var and a small sample size, and at low values of Var and a large sample size.
- The largest value for the increase in the DL of RT over the LYSFT (for a given MCM yield and Var) is significant [from about 45(%) to 80(%) in DL].
- Compared with ET, a considerable number of tests can be saved at a small increase in DL using the LYSFT. The LYSFT is more effective for high yield MCMs and for high variance in KGYs between strata.
- Compared with RT and RST, the LYSFT outperforms both of them, while RST outperforms RT just by a small amount.

VII. Simulation Results

Monte Carlo simulations have been performed to evaluate the validity and effectiveness of the proposed approach. Two thousand MCMs have been simulated (each MCM consists of 200 chips and has KGY of 0.9). Possible gains in value due to simulation without actual implementation should be noted within the given assumptions and the simulation has been driven with the given confidence level and interval in each case.

For the RST, each stratum is tested in a random order (i.e., the KGY of each stratum is not considered). Similarly, for the RT, each chip in the selected MCM is tested in a random order by ignoring the stratum. The simulation results are shown in Table II. In Table II, the differences between the analytical results of the proposed approaches (i.e., LYSFT, RST, RT) and the simulations results are given in %. The confidence interval of each simulation with 2000 sampled MCMs is in the range of $\pm 2.7\%$ to $\pm 16.1\%$.

VIII. Discussion and Conclusions

This paper has proposed a new testing approach for MCMs to achieve a high QL and to save a significant number of tests during assembly. In this paper, it has been shown that the stratification of MCMs due to the different nature and procurement of the chips can be exploited for testing. Unlike conventional RT, the proposed approach referred to as the LYSFT, takes into account the uneven KGY due to stratification to improve the QL

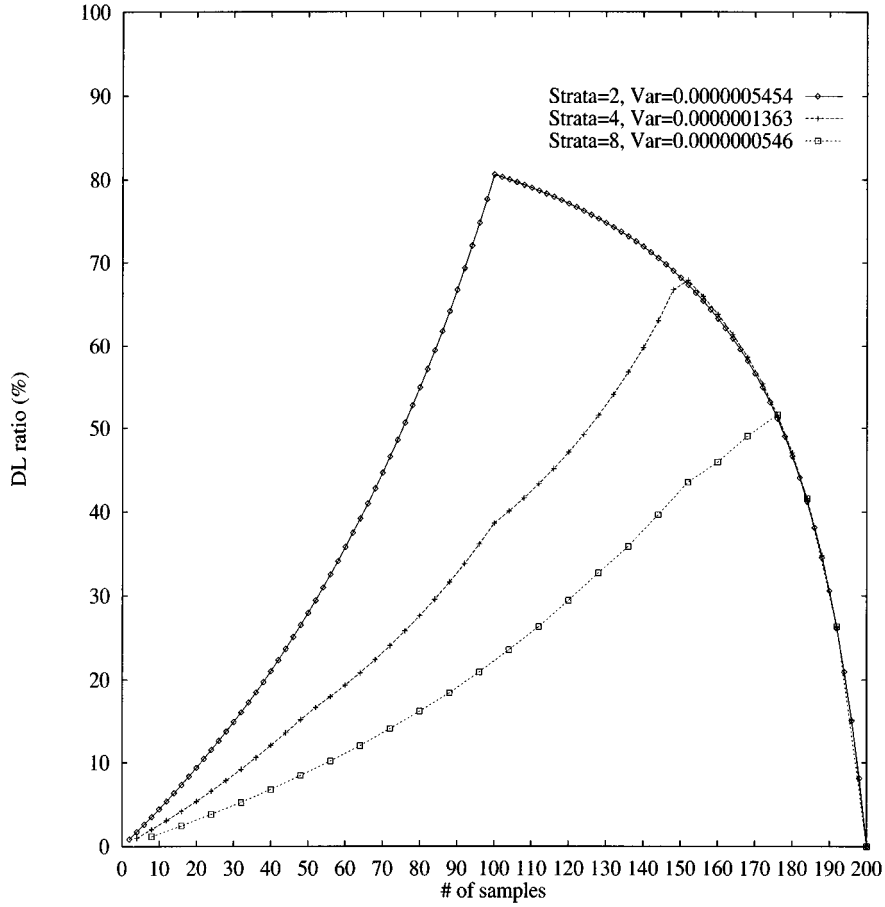

Fig. 7. DL ratio (RT versus LYSFT) by Stratified testing (at MCM Yield = 90%, FC = 90%).

(compared with conventional RT and RST). A Markov model has been proposed to evaluate the proposed approach under the assumption of independent failure of chips in the MCM.

In the LYSFT approach, the effect of the uneven KGY between strata has been analyzed with respect to the variance of KGY and the sample size. It is shown that the LYSFT approach significantly outperforms conventional RT and RST, and is competitive even with a conventional ET at a very small loss in QL by greedy (first) testing the chips in the stratum with lower KGY. Also, a new figure of merit to relate the cost of the testing process to the DL and the number of samples is proposed. This is a function of cost relative to the ET; the cost of the LYSFT is shown to outperform RT and RST for a given level of sample size.

Extensive parametric and cost analysis has been performed for comparing RT, RST, and ET. From the results of the parametric analysis, the LYSFT is shown to be more effective under a high MCM yield and high variance of KGY between strata. This has been further verified through Monte Carlo simulation. The performance of the proposed LYSFT can outperform RT by about 45%–80% improvement in QL and is viable even compared with a conventional ET for a significant reduction in the number of tests for an acceptable low loss in QL.

APPENDIX

The difference equations for the state diagram are as follows:

1) for the states in which the current chip is sampled for testing:

$$P(i, j, k, s) = P(i, j, k, s) + P(i-1, j, k, s)Y, \quad \text{for } i-1 \geq 0 \tag{5}$$

$$P(i, j, k, s) = P(i, j, k, s) + P(i, j-1, k, s)\overline{Y}C, \quad \text{for } j-1 \geq 0 \tag{6}$$

$$P(i, j, k, s) = P(i, j, k, s) + P(i, j, k-1, s)\overline{Y}\,\overline{C}, \quad \text{for } k-1 \geq 0 \tag{7}$$

where $P(i, j, k, s)$ represents the state probability of having i, j, k chips tested (and mounted) as good, bad, and escaped. Y, C represent the KGY and FC.

2) for the states in which the current chip is not sampled for testing:

$$P(i, j, k, s) = P(i, j, k, s) + P(i-1, j, k, s)Y, \quad \text{for } i-1 \geq 0 \tag{8}$$

$$P(i, j, k, s) = P(i, j, k, s) + P(i, j, k-1, s)\overline{Y}, \quad \text{for } k-1 \geq 0. \tag{9}$$

TABLE II
SIMULATION RESULTS AT MCM YIELD = 0.9

Sample size	$S = 4$, $Var = 0.1363 \times 10^{-6}$				
	Analytical	Simulation (difference%)	Confidence interval% 90%	95%	99%
16(LYSFT)	89,228	88,350(−0.9)	±2.7	±3.2	±4.2
16(RST)	93,144	92,700(−0.4)	±4.7	±5.7	±7.5
16(Random)	93,153	93,200(+0.0)	±3.2	±3.8	±5.1
112(LYSFT)	28,864	27,900(−3.3)	±5.7	±6.8	±9.0
112(RST)	46,184	48,300(+4.3)	±4.5	±5.4	±7.2
112(Random)	50,918	50,700(−0.4)	±3.7	±4.4	±5.8
192(LYSFT)	10,484	11,150(+5.9)	±10.3	±12.2	±16.1
192(RST)	14,222	13,700(−3.6)	±6.5	±7.8	±10.3
192(Random)	14,224	14,600(+2.5)	±5.7	±6.8	±9.0
200(Exhaustive)	10,478				

Sample size	$S = 8$, $Var = 0.0546 \times 10^{-6}$				
	Analytical	Simulation (difference%)	Confidence interval% 90%	95%	99%
16(LYSFT)	90,224	91,200(+1.0)	±2.8	±3.3	±4.4
16(RST)	92,490	91,900(−0.6)	±4.3	±5.1	±6.7
16(Random)	92,494	92,700(+0.2)	±3.3	±3.9	±5.1
112(LYSFT)	37,277	36,449(−2.2)	±7.0	±8.4	±11.0
112(RST)	47,668	48,600(+1.9)	±6.7	±8.0	±10.5
112(Random)	50,550	49,400(−2.2)	±5.6	±6.7	±8.8
192(LYSFT)	10,404	10,404(−1.9)	±5.7	±6.8	±9.0
192(RST)	14,119	13,500(−4.3)	±5.4	±6.4	±8.5
192(Random)	14,120	14,049(−0.5)	±9.4	±11.2	±14.7
200(Exhaustive)	10,401				

REFERENCES

[1] M. N. Ericson *et al.*, "Front-end module readout and control electronics for the PHENIX multiplicity vertex detector," *IEEE Trans. Nucl. Sci.*, pt. 1, vol. 45, pp. 833–837, June 1998.

[2] R. Caffrey, M. Cuviello, P. Hestnes, and H. Shaw, "A standard spacecraft data system on a chip: NASA Goddard Space Flight Center's Essential Services Node (ESN)," in *IEEE Proc. Aerospace Conf. 1997*, vol. 3, Feb. 1997, pp. 505–521.

[3] L. Breveglieri and V. Piuri, "A modular fault-tolerant approach to design a front-end microsystem for calorimetry at LHC," in *IEEE Instrum. Meas. Tech. Conf. 1994*, vol. 3, May 1994, pp. 1136–1139.

[4] A. Kourepenis and A. et al, "Performance of MEMS inertial sensors," in *IEEE Position Location and Navigation Symp.*, May 1994, pp. 1–8.

[5] J. K. Hagge and R. J. Wagner, "High-yield assembly of multichip modules through known-good IC's and effective test strategies," *Proc. IEEE*, vol. 80, pp. 1965–1994, Dec. 1992.

[6] T. Yamane, *Elementary Sampling Theory*. Englewood Cliffs, NJ: Prentice-Hall, 1967.

[7] C. M. Habiger and R. M. Lea, "Cost and delivery benefits of fault-tolerant multi-chip modules for massively parallel computing," in *Proc. IEEE Int. Workshop DFT VLSI Systems*, Venice, Italy, Oct. 1993.

[8] ——, "Reducing cost and ensuring on-time delivery of hybrid-WSI massively parallel computing modules," in *Proc. IEEE Int. Conf. Wafer Scale Integration*, San Francisco, CA, Jan. 1994, pp. 218–227.

[9] M. S. Abadir and A. R. Parikh *et al.*, "Analyzing multichip module testing strategies," *IEEE Design Test Comput.*, vol. 11, no. 1, pp. 40–52, 1994.

[10] M. Lubaszewski, M. Marzouki, and M. H. Touati, "A pragmatic test and diagnosis methodology for partially testable MCMs," in *Proc. IEEE MCMC*, Mar. 1994, pp. 108–113.

[11] MAD. P. Siewiorek and R. S. Swqrz, *Reliable Computer Systems, Design and Evaluation*, 2nd ed. Bedford: Digital, 1992.

[12] W. Jone, P. Gondalia, and A. Gutjahr, "Realizing a high measure of confidence for defect level analysis of random testing," *IEEE Trans. VLSI Syst.*, vol. 3, pp. 446–450, Sept. 1995.

[13] P. Gondalia, A. Gutjahr, and W. Jone, "Realizing a high measure of confidence for defect level analysis of random testing," in *Proc. IEEE Int. Test Conf.*, Sept. 1993, pp. 478–487.

[14] W. B. Jone, "Defect level estimation of circuit testing using sequential statistical analysis," *IEEE Trans. Computer-Aided Design*, vol. 12, pp. 336–348, Feb. 1993.

[15] M. Jacomino and R. David, "A new approach of test confidence estimation," in *Proc. Int. Symp. on Fault-Tolerant Comput.*, 1989, pp. 307–314.

[16] A. Majumdar and S. B. K. Vrudhula, "Fault coverage and test length estimation for random pattern testing," *IEEE Trans. Comput.*, vol. 44, pp. 234–247, Feb. 1995.

[17] S. R. Das and W. Jone, "On random testing for combinational circuits with a high measure of confidence," *IEEE Trans. Syst., Man, Cybern.*, vol. 22, pp. 748–754, July/Aug. 1992.

[18] N. Park, S. Kim, and F. Lombardi, "Modeling quality reduction of multichip module systems due to uneven fault-coverage and imperfect diagnosis," in *IEEE Int. Symp. Defect Fault Tolerance VLSI Syst.*, Nov. 1996.

[19] N. Park, F. Meyer, and F. Lombardi, "Quality-effective repair of multichip module systems," in *IEEE Int. Symp. Defect Fault Tolerance VLSI Systems*, Oct. 2000.

[20] S. K. Tewksbury and L. A. Hornak, "The legacy of WSI research in MCM test/repair strategies," in *IEEE Int. Conf. WSI*, Jan. 1992, pp. 135–144.

[21] A. Flint, "Testing multichip modules," *IEEE Spectrum*, vol. 31, pp. 59–62, Mar. 1994.

[22] C. Bolchini, G. Buonanno, and G. et al, "A wafer level testability approach based on an improved scan insertion technique," *IEEE Trans. Comp., Packag., Manufact., Technol. B*, vol. 18, pp. 438–447, Aug. 1995.

[23] S. Chiu and C. A. Papachristou, "A partial scan cost estimation method at the system level," in *IEEE ICCD*, Oct. 1995, pp. 146–150.

[24] V. Chickermane and J. H. Patel, "An optimization based approach to the partial scan design problem," in *IEEE ITC*, Sept. 1990, pp. 377–386.

[25] Y. Zorian, "A structured testability approach for multi-chip modules based on BIST and boundary-scan," *IIEEE Trans. Comp., Packag., Manufact., Technol. B*, vol. 17, pp. 283–290, Aug. 1994.

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